REPLY UNDER 37 C.F.R. 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2634

Amendment of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A method of testing a circuit which outputs serial information, comprising the steps of:

instructing the circuit to output a serial bitstream that conforms to a defined bit sequence;

sampling a plurality of selected bits in said bitstream to determine a state of each of said selected bits, each of said selected bits being separated from other selected bits in said bitstream by at least one nonselected bit; and

determining whether said state obtained by said sampling for each said selected bit conforms to an expected state therefor according to said defined bit sequence; wherein said defined bit sequence includes N successive subsequences, and including the step of shifting sampling times relative to said bitstream by one bit width at the end of each said subsequence.

2. (original) A method according to Claim 1, wherein said sampling step includes the step of sampling every Nth bit of said bitstream.

3. (canceled)

4. (original) A method according to Claim 3, wherein said circuit also outputs a serial bit sequence representing a clock synchronized to said serial bitstream, said serial bitstream having a number of bits per second which is N times a frequency of said clock, said sampling being carried out in a manner synchronized to said clock, and said step of shifting sampling times being carried out by changing said serial bit sequence in a manner which effectively shifts the phase of said clock relative to said serial bitstream.

5. (original) A method according to Claim 2, wherein said defined bit sequence includes a plurality of successive groups of N bits, each said group having one bit which corresponds to a respective one of said selected bits in said serial bitstream, and having N-1 further bits which each have a logical state that is the inverse of the logical state of said one bit.

6. (original) An apparatus, comprising:

a circuit operable to output serial information;

a control section operable to instruct said circuit to output a serial bitstream that conforms to a defined bit sequence;

a sampling section operable to sample a plurality of selected bits in said bitstream to determine a state of each of said selected bits, each of said selected bits being separated from other selected bits in said bitstream by at least one nonselected bit; and

an error detecting section operable to determine whether said state obtained by said sampling section for each said selected bit conforms to an expected state therefor according to said defined bit sequence,

wherein said control section is operable to cause said defined bit sequence to include N successive subsequences, and wherein said sampling section is operable to shift sampling times relative to said bitstream by one bit width at the end of each said subsequence..

7. (original) An apparatus according to Claim 6, wherein said sampling section is operable to sample every Nth bit in said serial bitstream.

8. (canceled)

9. (original) An apparatus according to Claim 8, wherein said circuit includes a data serializer which has an N-bit parallel input and which generates said serial bitstream by serially outputting the bits of successive N-bit words supplied to said parallel input thereof;

and wherein said control section is operable to supply a sequence of N-bit words to said parallel input of said serializer during each said subsequence.

10. (original) An apparatus according to Claim 9, wherein said control section includes a portion which is operable to generate a predetermined sequence of N-bit words N successive times which each correspond to a respective said subsequence, and includes a decoder which is operable to effect a closed rotate of said bits of each said N-bit word by a number of bits which is different during each said subsequence, the rotated N-bit words from said decoder being supplied to said parallel input of said serializer.

11. (original) An apparatus according to Claim 10, wherein said control section includes a multiplexer having an N-bit first input to which is applied a predetermined N-bit word, having an N-bit second input to which is applied the rotated N-bit words from said decoder, and having an N-bit output which is coupled to said parallel input of said serializer; and wherein said control section is operable to cause said multiplexer to select said first input during a normal operational mode and to select said second input during a test operational mode.

12. (original) An apparatus according to Claim 8, wherein said circuit also outputs a serial bit sequence representing a clock synchronized to said serial bitstream, the number of bits per second in said serial bitstream being N times the frequency of said clock, said sampling section being operable to carry out said sampling in a manner synchronized to said clock, and said control section being operable to effect said shifting of said sampling times by changing said serial bit sequence in a manner corresponding to a change in the phase of said clock relative to said serial bitstream.

13. (original) An apparatus according to Claim 12, wherein said circuit includes a clock serializer which has an N-bit parallel input, and which generates said serial bit sequence by serially outputting the bits of successive N-bit words supplied to said parallel input thereof; and wherein said control section includes a portion operable to continuously supply a selected N-bit word to said parallel input of said serializer throughout each said subsequence, and to effect said change in the phase of said clock by changing the selected N-bit word at the end of each said subsequence.

14. (original) An apparatus according to Claim 13, wherein said control section includes a multiplexer having an N-bit first input to which is applied a predetermined N-bit word, having an N-bit second input to which is applied the selected N-bit words from said portion of said control section, and having an N-bit output which is coupled to said parallel input of said serializer; and wherein said control section is operable to cause said multiplexer to select said first input during a normal operational mode and to select said second input during a test operational mode.

15. (original) An apparatus according to Claim 7, wherein said control section is operable to use as said defined bit sequence a plurality of successive groups of N bits, each said group including one bit that corresponds to a respective one of said selected bits in said serial bitstream, and including N-1 further bits that each have a logical state which is the inverse of the logical state of said one bit.

16. (original) An apparatus according to Claim 6, wherein said error detecting section includes a pattern generator operable to produce a serial bit sequence which represents successive said expected states of said selected bits in said bitstream, and includes a comparator operable to successively compare said states obtained by said sampling section for said selected bits to said expected states in said bit sequence from said pattern generator, said comparator having an output which is coupled to an output port of said apparatus.

17. (original) An apparatus according to Claim 6, wherein said control circuit operates in response to an input clock from an input port; and wherein said error detecting section includes a counter operable to count pulses of said input clock, said counter having an output which is coupled to an output port of said apparatus.

18. (Newly added) An integrated transmitter circuit, comprising:

an output circuit operable to output serial information, wherein said output circuit includes a data serializer which has an N-bit parallel input and which generates said serial bitstream by serially outputting the bits of successive N-bit words supplied to said parallel input thereof; and wherein said control section is operable to supply a sequence of N-bit words to said parallel input of said serializer during each said subsequence;

a control section operable to instruct said circuit to output a serial bitstream that conforms to a defined bit sequence;

a sampling section operable to sample a plurality of selected bits in said bitstream from said data serilizer to determine a state of each of said selected bits, each of said selected bits being separated from other selected bits in said bitstream by at least one nonselected bit; and

an error detecting section operable to determine whether said state obtained by said sampling section for each said selected bit conforms to an expected state therefor according to said defined bit sequence.

19. (newly added) A transmitter circuit according to Claim 18, wherein said sampling section is operable to sample every Nth bit in said serial bitstream and wherein said control section is operable to cause said defined bit sequence to include N successive subsequences, and wherein said sampling section is operable to shift sampling times relative to said bitstream by one bit width at the end of each said subsequence.

20. (newly added) An transmitter circuit according to Claim 19, wherein said control section includes a portion which is operable to generate a predetermined sequence of N-bit words N successive times which each correspond to a respective said subsequence, and includes a decoder which is operable to effect a closed rotate of said bits of each said N-bit word by a number of bits which is different during each said subsequence, the rotated N-bit words from said decoder being supplied to said parallel input of said serializer.

21. (newly added) A transmitter circuit according to Claim 20, wherein said control section includes a multiplexer having an N-bit first input to which is applied a predetermined N-bit word, having an N-bit second input to which is applied the rotated N-bit words from said decoder, and having an N-bit output which is coupled to said parallel input of said serializer; and wherein said control section is operable to cause said multiplexer to select said first input during a normal operational mode and to select said second input during a test operational mode.

22. (newly added) A transmitter circuit according to Claim 18, wherein said error detecting section includes a pattern generator operable to produce a serial bit sequence which represents successive said expected states of said selected bits in said bitstream, and includes a comparator operable to successively compare said states obtained by said sampling section for said selected bits to said expected states in said bit sequence from said pattern generator, said comparator having an output which is coupled to an output port of said apparatus.